



Attorney Docket No.: CYPR-CD00183

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Warren Snyder

Serial No.: 09/975,104

Group Art Unit:

Filed: 10/10/01

Examiner:

Title: CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING FPGA
FOR IN-CIRCUIT EMULATION**RECEIVED**

JAN 23 2003

Technology Center 2100

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
AB	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
	C						
	D						
	E						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	F							
	G							
	H							

Related Pending US Patent Applications

Examiner Initial	No.	Docket Number, Title, Filing Date, Serial Number & Inventors
AB	I	CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE"; 10/10/01; 09/975,115; Snyder et al.
	J	CYPR-CD00184; "HOST TO FPGA INTERFACE IN AN IN-CIRCUIT EMULATION SYSTEM"; 10/10/01; 09/975,105; Nemecek
	K	CYPR-CD00185; "EMULATOR CHIP-BOARD ARCHITECTURE AND INTERFACE"; 10/1/01; 09/975,030; Snyder et al.
	L	CYPR-CD00186; "METHOD FOR BREAKING EXECUTION OF TEST CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS"; 10/10/01; 09/975,338; Nemecek et al.
Examiner AB Broda		Date Considered 3/3/2005

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.